IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	Docket No.: 6161.0111.US
Ji-Yong PARK, et al.	Confirmation No.: 1632
Application No.: 10/779,781	Group Art Unit: 2815
Filed: February 18, 2004	Examiner: LANDAU, Matthew C.

For: **FLAT PANEL DISPLAY DEVICE WITH POLYCRYSTALLINE SILICON THIN FILM TRANSISTOR**

Mail Stop 16
Commissioner for Patents
P.O. BOX 1450
Alexandria, VA 22313-1450

REQUEST FOR REFUND

Sir:

Applicants hereby request a refund in the amount of $200.00 in connection with the above-referenced patent application. The following are the statement of facts:

- On July 17, 2006, Applicant filed a Reply and Amendment Under 37 C.F.R. §1.111 in response to a Non-Final Office Action (see Exhibit A).
- On August 14, 2006, Applicants received a Monthly Statement of Deposit Account dated July 31, 2006 for deposit account no. 50-3698 (see Exhibit B). The Statement indicates that on July 25, 2006, the amount of $200.00 was charged to Applicants' deposit account to cover the fee for one additional independent claim.
- Upon receipt of the Statement of Account, Applicants accessed the above-mentioned application through PAIR, and obtained a copy of the Fee Worksheet and Index of Claims (see Exhibit C). The Index of Claims indicates that claims 4, 6, 14, 27, 37, 47 and 48 are independent claims; however, claim 6 is not an independent claim. Therefore, the $200.00 fee for an additional independent claim should not have been charged to Applicants' deposit account no. 50-3698.

Based on the facts above, a refund in the amount of $200.00 is in order. Applicants request that the refund of $200.00 be deposited into Applicants' deposit account No. 50-3698.

Respectfully Submitted,

/hae-chan park/

Hae-Chan Park
Reg. No. 50,114

Date: August 15, 2006

CUSTOMER NUMBER: 58027
HCP/BYC/kbs

EXHIBIT A

Reply and Amendment Under 37 C.F.R. §1.111 filed on July 17, 2006

Electronic Acknowledgement Receipt

EFS ID:	1115231
Application Number:	10779781
Confirmation Number:	1632
Title of Invention:	Flat panel display device with polycrystalline silicon thin film transistor
First Named Inventor:	Ji-Yong Park
Customer Number:	58027
Filer:	Hae-Chan Park/Wayne Helge
Filer Authorized By:	Hae-Chan Park
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part	Pages
1		Reply_filed_07-17-06.pdf	158703	yes	20

	Doc Desc	Start	End
	Amendment - After Non-Final Rejection	1	1
	Claims	2	12
	Applicant Arguments/Remarks Made in an Amendment	13	20

Warnings:	
Information:	
Total Files Size (in bytes):	158703

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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For: **FLAT PANEL DISPLAY DEVICE WITH POLYCRYSTALLINE SILICON THIN FILM TRANSISTOR**

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY AND AMENDMENT UNDER 37 C.F.R. § 1.111

Sir:

In response to the Non-Final Office Action mailed April 20, 2006 ("Office Action"), Applicants respectfully request reconsideration of the application in view of the following Amendments and Remarks.

Amendments to the Claims begin on page 2.

Remarks begin on page 13.

Applicants believe that no extensions of time are required at this time. If extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned for under 37 C.F.R. § 1.136(a). Applicants believe that no further fees for net addition of claims are required at this time. Any fees required for further extensions of time and any fees for the net addition of claims are hereby authorized to be charged to our **Deposit Account No. 50-3698 (H.C. Park & Associates, PLC).**

AMENDMENTS TO THE CLAIMS

Please **AMEND** claims 3, 4, 8, 13, 47, and 48 as shown below.

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Cancelled)

2. (Withdrawn) The flat panel display device with polycrystalline silicon thin film transistor according to claim 1, wherein a shape of the grains of polycrystalline silicon is anisotropic, and the grain boundaries are primary grain boundaries.

3. (Currently Amended) The flat panel display device with polycrystalline silicon thin film ~~transistor~~ transistors according to claim 4, wherein a shape of the grains of polycrystalline silicon is anisotropic, and the grain boundaries include side grain boundaries of anisotropic grains.

4. (Currently Amended) A flat panel display device with polycrystalline silicon thin film ~~transistor~~ transistors, comprising:

a pixel portion divided by gate lines and data lines and comprising [[a]] thin film transistors driven by signals applied by the gate lines and data lines; and

a driving circuit portion comprising [[a]] thin film transistors connected to the gate lines and data lines respectively to apply signals to the pixel portion,

wherein an average number of grain boundaries of polycrystalline silicon formed in an active channel region of each ~~the~~ thin film transistor[[s]] installed at the driving circuit portion and meet a current direction line is at least one or more less than an average number of grain

boundaries of polycrystalline silicon formed in an active channel region of each ~~the~~ thin film transistor installed at the pixel portion and meet a current direction line for a unit area of active channels,

wherein the polycrystalline silicon grain boundaries formed in the active channel regions of each ~~the one or more~~ thin film transistor[[s]] installed at the driving circuit portion include primary polycrystalline silicon grain boundaries that are inclined to the current direction line at an angle of about – 45 to 45°,

wherein the polycrystalline silicon grain boundaries formed in the active channel regions of each ~~the~~ thin film transistor installed at the pixel portion include primary polycrystalline silicon grain boundaries that are inclined to the current direction line at an angle of about – 45 to 45°, and

wherein the active channel of each ~~the~~ thin film transistor installed at the pixel portion is longer than the active channel of each ~~the~~ thin film transistor installed at the driving circuit portion.

5. (Withdrawn) The flat panel display device with polycrystalline silicon thin film transistor according to claim 1, wherein:

the polycrystalline silicon grain boundaries formed in active channel regions of the one or more thin film transistors installed at the driving circuit portion are arranged in such a way that the polycrystalline silicon grain boundaries are inclined to the current direction line at an angle of 45 to 135°; and

the polycrystalline silicon grain boundaries formed in active channel regions of the thin film transistor installed at the pixel portion are arranged in such a way that the polycrystalline silicon grain boundaries are inclined to the current direction line at an angle of – 45 to 45°.

6. (Withdrawn) The flat panel display device with polycrystalline silicon thin film transistor according to claim 1, wherein:

the polycrystalline silicon grain boundaries formed in active channel regions of the one or more thin film transistors installed at the driving circuit portion are arranged in such a way that the polycrystalline silicon grain boundaries are inclined to the current direction line at an angle of – 45 to 45°;

the polycrystalline silicon grain boundaries formed in active channel regions of the thin film transistor installed at the pixel portion are arranged in such a way that the polycrystalline silicon grain boundaries are inclined to the current direction line at an angle of – 45 to 45°; and

the length of the active channels of the thin film transistor installed at the pixel portion is the same as length of the active channels of the thin film transistor installed at the driving circuit portion.

7. (Withdrawn) The flat panel display device with polycrystalline silicon thin film transistor according to claim 2, wherein the polycrystalline silicon is fabricated by a sequential lateral solidification method.

8. (Currently Amended) The flat panel display device with polycrystalline silicon thin film ~~transistor~~ transistors according to claim 3, wherein the polycrystalline silicon is fabricated by a metal induced lateral crystallization method.

9. (Withdrawn) The flat panel display device with polycrystalline silicon thin film transistor according to claim 1, wherein shape of the grains of polycrystalline silicon is isotropic.

10. (Withdrawn) The flat panel display device with polycrystalline silicon thin film transistor according to claim 7, wherein a length of the active channels of the thin film transistor

installed at the pixel portion is the same as length of the active channels of the one or more thin film transistors installed at the driving circuit portion.

11. (Withdrawn) The flat panel display device with polycrystalline silicon thin film transistor according to claim 7, wherein the polycrystalline silicon is formed by eximer laser annealing.

12. (Withdrawn) The flat panel display device with polycrystalline silicon thin film transistor according to claim 1, wherein the average grain size of polycrystalline silicon grains included in active channel region of a gate in the driving circuit portion is larger than that of polycrystalline silicon grains included in active channel region of a gate in the pixel portion.

13. (Currently Amended) The flat panel display device with polycrystalline silicon thin film ~~transistor~~ transistors according to claim 4, wherein the flat panel display device is one of an organic ~~electroluminscent~~ electroluminescent device and a liquid crystal display device.

14. (Withdrawn) A flat panel display device with polycrystalline silicon thin film transistor comprising:

a switching thin film transistor for transmitting data signals; and

a driving thin film transistor for driving the organic electroluminescent device so that a certain amount of current flows through organic electroluminescent device according to the data signals, wherein the average number of grain boundaries of polycrystalline silicon which are formed in active channel regions of the driving thin film transistor and meet a current direction line is at least one or more greater than the average number of grain boundaries of polycrystalline silicon which are formed in active channel regions of the switching thin film transistor and meet a current direction line for a unit area of active channels.

15. (Withdrawn) The flat panel display device with polycrystalline silicon thin film transistor according to claim 14, wherein a shape of the grains of polycrystalline silicon is anisotropic, and the grain boundaries are primary grain boundaries.

16. (Withdrawn) The flat panel display device with polycrystalline silicon thin film transistor according to claim 14, wherein a shape of the grains of polycrystalline silicon is anisotropic, and the grain boundaries are side grain boundaries of anisotropic grains.

17. (Withdrawn) The flat panel display device with polycrystalline silicon thin film transistor according to claim 14, wherein:

the polycrystalline silicon grain boundaries formed in active channel regions of the switching thin film transistor are arranged in such a way that the polycrystalline silicon grain boundaries are inclined to the current direction line at an angle of – 45 to 45°;

the polycrystalline silicon grain boundaries formed in active channel regions of the driving thin film transistor are arranged in such a way that the polycrystalline silicon grain boundaries are inclined to the current direction line at an angle of –45 to 45°; and

the length of the active channels of the driving thin film transistor is longer than length of the active channels of the switching thin film transistor.

18. (Withdrawn) The flat panel display device with polycrystalline silicon thin film transistor according to claim 14, wherein:

the polycrystalline silicon grain boundaries formed in active channel regions of the switching thin film transistor are arranged in such a way that the polycrystalline silicon grain boundaries are inclined to the current direction line at an angle of 45 to 135°; and

the polycrystalline silicon grain boundaries formed in active channel regions of the driving thin film transistor are arranged in such a way that the polycrystalline silicon grain boundaries are inclined to the current direction line at an angle of – 45 to 45°.

19. (Withdrawn) The flat panel display device with polycrystalline silicon thin film transistor according to claim 14, wherein:

the polycrystalline silicon grain boundaries formed in active channel regions of the switching thin film transistor are arranged in such a way that the polycrystalline silicon grain boundaries are inclined to the current direction line at an angle of – 45 to 45°;

the polycrystalline silicon grain boundaries formed in active channel regions of the driving thin film transistor are arranged in such a way that the polycrystalline silicon grain boundaries are inclined to the current direction line at an angle of – 45 to 45°; and

the length of the active channels of the driving thin film transistor is the same as length of the active channels of the switching thin film transistor.

20. (Withdrawn) The flat panel display device with polycrystalline silicon thin film transistor according to claim 15, wherein the polycrystalline silicon is fabricated by a sequential lateral solidification method.

21. (Withdrawn) The flat panel display device with polycrystalline silicon thin film transistor according to claim 16, wherein the polycrystalline silicon is fabricated by a metal induced lateral crystallization method.

22. (Withdrawn) The flat panel display device with polycrystalline silicon thin film transistor according to claim 14, wherein shape of the grains of polycrystalline silicon is isotropic.

23. (Withdrawn) The flat panel display device with polycrystalline silicon thin film transistor according to claim 22, wherein a length of the active channels of the driving thin film transistor is the same as length of the active channels of the switching thin film transistor.

24. (Withdrawn) The flat panel display device with polycrystalline silicon thin film transistor according to claim 22, wherein the polycrystalline silicon is formed by eximer laser annealing.

25. (Withdrawn) The flat panel display device with polycrystalline silicon thin film transistor according to claim 14, wherein the average grain size of polycrystalline silicon grains included in active channel region of a gate in the switching thin film transistor is larger than that of polycrystalline silicon grains included in active channel region of a gate in the driving thin film transistor.

26. (Withdrawn) The flat panel display device with polycrystalline silicon thin film transistor according to claim 14, wherein the flat panel display device is one of an organic electroluminscent device and a liquid crystal display device.

27. (Withdrawn) A CMOS thin film transistor characterized in that a P type thin film transistor and an N type thin film transistor have a different number of primary grain boundaries of polycrystalline silicon included in active channel regions, and the number of grain boundaries included in the P type thin film transistor is at least one or more less than the number of grain boundaries included in the N type thin film transistor.

28. (Withdrawn) The CMOS thin film transistor according to claim 27, wherein channel length of the P type thin film transistor is the same as that of the N type thin film transistor.

29. (Withdrawn) The CMOS thin film transistor according to claim 27, wherein the primary grain boundaries of polycrystalline silicon included in the active channel regions of the N type thin film transistor and P type thin film transistor are perpendicular to a current flow direction.

30. (Withdrawn) The CMOS thin film transistor according to claim 27, wherein the polycrystalline silicon is fabricated by a sequential lateral solidification crystallization method.

31. (Withdrawn) The CMOS thin film transistor according to claim 27, wherein the primary grain boundaries are not included in the P type thin film transistor.

32. (Withdrawn) The CMOS thin film transistor according to claim 27, wherein the number of primary grain boundaries included in the P type thin film transistor is 2 or less.

33. (Withdrawn) The CMOS thin film transistor according to claim 32, wherein the number of primary grain boundaries included in the N type thin film transistor is 6, and the number of primary grain boundaries included in the P type thin film transistor is 2.

34. (Withdrawn) The CMOS thin film transistor according to claim 27, wherein the CMOS thin film transistor includes one of an LDD structure an off-set structure.

35. (Withdrawn) A display device using the CMOS thin film transistor of claim 27.

36. (Withdrawn) The display device according to claim 35, wherein the display device is one of a liquid crystal display device and an organic electroluminescent display device.

37. (Withdrawn) A flat panel display device comprising green, red and blue pixel regions, and driving thin film transistor for driving each of the pixels having the same length and width of active channels, wherein the number of grain boundaries of polycrystalline silicon

included in active channel regions of the driving thin film transistor is different from each other for each pixel.

38. (Withdrawn) The flat panel display device according to claim 37, wherein the green pixel region has the largest number of the primary grain boundaries of polycrystalline silicon, and the red pixel region and the blue pixel region have the same number of the primary grain boundaries of polycrystalline silicon.

39. (Withdrawn) The flat panel display device according to claim 37, wherein the number of the primary grain boundaries of polycrystalline silicon is increased in the order of green, blue and red pixel regions.

40. (Withdrawn) The flat panel display device according to claim 37, wherein the green pixel region and the blue pixel region have the same number of the primary grain boundaries of polycrystalline silicon, and the red pixel region has the smallest number of the primary grain boundaries of polycrystalline silicon.

41. (Withdrawn) The flat panel display device according to claim 37, wherein the grain boundaries are perpendicular to current flowing direction in active channel regions of each driving thin film transistor.

42. (Withdrawn) The flat panel display device according to claim 41, wherein the grain boundaries are primary grain boundaries.

43. (Withdrawn) The flat panel display device according to claim 41, wherein the grain boundaries are side grain boundaries of anisotropic grains.

44. (Withdrawn) The flat panel display device according to claim 43, wherein the flat panel display device has the smallest number of primary grain boundaries included in active channel regions of driving thin film transistor of the green pixel region.

45. (Withdrawn) The flat panel display device according to claim 44, wherein the number of primary grain boundaries included in active channel regions of driving thin film transistor of the blue pixel region is the same as or less than the number of primary grain boundaries included in active channel regions of driving thin film transistor of the red pixel region.

46. (Withdrawn) The flat panel display device according to claim 37, wherein the flat panel display device is one of a liquid crystal display device, an inorganic electroluminescent device and an organic electroluminescent device.

47. (Currently Amended) A flat panel display device with polycrystalline silicon thin film ~~transistor~~ transistors, comprising:

a switching thin film transistor for transmitting data signals; and

a driving thin film transistor for driving an organic electroluminescent device so that a certain amount of current flows through the organic electroluminescent device according to the data signals,

wherein an average number of grain boundaries of polycrystalline silicon which are formed in an active channel region of the driving thin film transistor and meet a current direction line is more than zero and at least one or more less than an average number of grain boundaries of polycrystalline silicon which are formed in an active channel region of the switching thin film transistor and meet a current direction line for a unit area of an active channel.

48. (Currently Amended) A flat panel display device with polycrystalline silicon thin film ~~transistor~~ transistors, comprising:

a pixel portion divided by gate lines and data lines and equipped with [[a]] thin film transistors driven by signals applied by the gate lines and data lines; and

a driving circuit portion comprising [[a]] thin film transistors connected to the gate lines and data lines respectively to apply signals to the pixel portion,

wherein [[the]] each thin film transistor at the driving circuit portion includes an average number of grain boundaries of polycrystalline silicon formed in an active channel region that meet a current direction line is more than zero and at least one less than an average number of grain boundaries of polycrystalline silicon formed in an active channel region of [[the]] each thin film transistor installed at the pixel portion that meet a current direction line for a unit area of an active channel.

REMARKS

By this amendment, claims 3, 4, 8, 13, 47, and 48 have been amended. Accordingly, claims 3, 4, 8, 13, 47, and 48 are currently pending in the application, of which claims 4, 47, and 48 are independent claims.

Applicants appreciate the indication that claims 3, 4, 8, and 13 contain allowable subject matter.

Applicants respectfully submit that the above amendments do not add new matter to the application and are fully supported by the specification. Support for the amendments may be found at least in FIGS. 4(A) & (B), 5(A) & (B), 6(A) & (B), 11(A) & (B), 12(A) & (B), and 13(A) & (B)).

In view of the above amendments and the following Remarks, Applicants respectfully request reconsideration and timely withdrawal of the pending objections and rejections for the reasons discussed below.

Claim Objection

In the Office Action, claims 3, 4, 18, 47 and 48 were objected to as containing informalities. Applicants respectfully believe that the Examiner meant to indicate that claims 3, 4, 8, 13, 47, and 48 contained informalities.

Claims 3, 4, 8, 13, 47, and 48 have been amended to correct such informalities. This amendment is made for the sole purpose of correcting such informalities. This amendment is not made for the purpose of avoiding prior art or narrowing the claimed invention, and no change in claim scope is intended. Therefore Applicants do not intend to relinquish any subject matter by these amendments. Applicants respectfully submit that claims 3, 4, 8, 13, 47, and 48, as amended, overcome the stated objection. Accordingly, Applicants respectfully request withdrawal of the objection for claims 3, 4, 8, 13, 47, and 48.

Therefore, claims 3, 4, 8, and 13 are now in condition for allowance.

Rejections Under 35 U.S.C. § 112, second paragraph

Claims 47 and 48 stand rejected under 35 U.S.C. § 112, second paragraph as being indefinite. Applicants respectfully traverse this rejection for at least the following reasons.

Applicants respectfully disagree that the limitations for "an average number of grain boundaries of polycrystalline silicon" render the claim indefinite. Each active channel region of each TFT includes a plurality of primary and secondary grain boundaries. Therefore, each active channel region of each TFT includes more than one grain boundary, where an average number of grain boundaries of polycrystalline silicon could be determined. Accordingly, Applicants respectfully believe that the claim limitation for "an average number of grain boundaries of polycrystalline silicon" is particular and distinct with regard to the subject matter of the present invention (See particularly FIGS. 4(A) & (B), 5(A) & (B), 6(A) & (B), 11(A) & (B), 12(A) & (B), and 13(A) & (B)); See specification at least at page 16, paragraph [0075] and [0076], pages 17 and 18, paragraph [0080], and page 22, paragraph [0102]).

Accordingly, Applicants respectfully request withdrawal of the 35 U.S.C. § 112, second paragraph rejection of claims 47 and 48.

Rejections Under 35 U.S.C. § 102

Claim 48 stands rejected under 35 U.S.C. § 102(b) as being allegedly anticipated by U.S. Patent No. 5,614,733 issued to Zhang, *et al.* ("Zhang").

Claim 48 also stands rejected under 35 U.S.C. § 102(b) as being allegedly anticipated by U.S. Patent No. 5,705,829 issued to Miyanaga, *et al.* ("Miyanaga"). Applicants respectfully traverse this rejection for at least the following reasons.

In order for a rejection under 35 U.S.C. § 102(b) to be proper, a single reference must disclose every claimed feature. To be patentable, a claim need only recite a single novel feature that is not disclosed in the cited reference. Thus, the failure of a cited reference to disclose one or more claimed features renders the 35 U.S.C. § 102(b) rejection improper.

Claim 48, as amended, recites *inter alia*:

> "A flat panel display device with polycrystalline silicon thin film transistors, comprising...wherein each thin film transistor at the driving circuit portion includes an average number of grain boundaries of polycrystalline silicon formed in an active channel region that meet a current direction line is more than zero and at least one less than an average number of grain boundaries of polycrystalline silicon formed in an active channel region of each thin film transistor installed at the pixel portion that meet a current direction line for a unit area of an active channel."

With respect to Zhang, Applicants respectfully submit that Zhang fails to teach or suggest such features. The Examiner indicates that it would have been "inherent that the average number of grain boundaries in the driving TFT that meet a direction line is at least one less than the average number grain boundaries in the pixel TFT that meet a current line direction" (See Office Action, on pages 4 and 5).

In relying upon the theory of inherency, the Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the prior art. *Ex parte Tanksley*, 37 USPQ2d 1382, 1385 (Bd. Pat. App. & Int'f 1994).

"To establish inherency, the extrinsic evidence, 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill in the art." *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d, 1949, 1950-51 (Fed. Cir. 1999) (citations omitted).

Applicants respectfully submit that the Examiner has failed to meet the burden of illustrating the claimed structural limitations are inherent. Further, the Examiner fails to provide

a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from Zhang. The Examiner cites the teachings of Zhang for the crystallinity of portions of the silicon film 12a, which are located under the silicon nickel film 13, are better than the crystallinity of the silicon film 12b in the other regions because the nickel promoted crystallization (See col. 8, lines 54-62), incorrectly concluding that the crystallinity of the portions used to make the channels of the driving TFT is greater than the crystallinity of the portions used to make the channels of the pixel TFT (See Office Action, on page 4). The Examiner concludes that it would have been inherent that the average number of grain boundaries that meet the current direction in the driving TFTs is more than zero, but at least one less than that of the pixel TFTs. Applicants respectfully submit that one of ordinary skill in the art would not have recognized that the claimed limitations of the present invention would necessarily flow from the teachings of Zhang cited by the Examiner.

Applicants respectfully submit that it appears that the Examiner's conclusions are based on a hindsight consideration of Applicants' claimed limitations, not on a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from Zhang. Accordingly, Zhang fails to teach each and every claimed feature of the present invention, as disclosed in amended claim 48.

Similar to the reasons noted above with respect to Zhang, Applicants respectfully submit that Miyanaga fails to teach or suggest such features. Applicants further respectfully submit that the Examiner has failed to meet the burden of illustrating the claimed structural limitations are inherent. Further, the Examiner fails to provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from Miyanaga. The requirements for an inherency rejection are provided above. The Examiner cites the teachings of Miyanaga for the direction of grain boundaries in the channel of

the driving TFT and the direction of grain boundaries in the channel of the pixel TFT (See Office action, on page 5; See Miyanaga, col. 2, lines 30-37). From these teachings in Miyanaga, the Examiner concludes that it would have been inherent that the average number of grain boundaries that meet the current direction in the driving TFTs is more than zero, but at least one less than that of the pixel TFTs. Applicants respectfully submit that the Examiner has not satisfied the burden required for establishing inherency. Further, Applicants respectfully submit that one of ordinary skill in the art would not have recognized that the claimed limitations of the present invention would necessarily flow from the teachings of Miyanaga cited by the Examiner.

Applicants respectfully submit that it appears that the Examiner's conclusions are based on a hindsight consideration of Applicants' claimed limitations, not on a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from Miyanaga. Accordingly, Miyanaga fails to teach each and every claimed feature of the present invention, as disclosed in amended claim 48.

Accordingly, Applicants respectfully request withdrawal of the 35 U.S.C. § 102(b) rejection of claim 48. Since none of the other prior art of record discloses or suggests all the features of the claimed invention, Applicants respectfully submit that independent claim 48, and all the claims that depend therefrom, are allowable.

Rejections Under 35 U.S.C. § 103

Claim 47 stands rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over U. S. Patent Publication No. 2004/0079944 issued to Hiroshima, *et al.* ("Hiroshima") in view of Zhang. Applicants respectfully traverse this rejection for at least the following reasons.

Claim 47 also stands rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Hiroshima in view of Miyanaga. Applicants respectfully traverse this rejection for at least the following reasons.

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the reference or references, when combined, must disclose or suggest all of the claim limitations. The motivation to modify the prior art and the reasonable expectation of success must both be found in the prior art and not based upon a patent applicant's disclosure. *See in re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

The examiner has failed to establish a prima facie case of obviousness. Assuming *arguendo* that the references may be combined and a reasonable expectation of success exists, the combined references do not disclose or suggest all of the claim limitations.

Claim 47, as amended, recites *inter alia*:

> "A flat panel display device with polycrystalline silicon thin film transistors, comprising...wherein an average number of grain boundaries of polycrystalline silicon which are formed in an active channel region of the driving thin film transistor and meet a current direction line is more than zero and at least one or more less than an average number of grain boundaries of polycrystalline silicon which are formed in an active channel region of the switching thin film transistor and meet a current direction line for a unit area of an active channel."

Applicants respectfully submit that Hiroshima fails to teach or suggest such features. As noted by the Examiner, Hiroshima fails to teach or suggest the specific limitations regarding the average number of grain boundaries in the channel regions of the switching and driving TFTs (See Office Action, on pages 6-8). As noted above with respect to claim 48, Zhang fails to teach or suggest such claimed features. Accordingly, Zhang fails to cure the deficiencies of Hiroshima. Accordingly, Hiroshima in view of Zhang fails to teach or suggest each and every claimed feature of the present invention, as disclosed in amended claim 47.

With respect to Miyanaga, Applicants further submit, as stated above, Miyanaga fails to teach or suggest such claimed features. Accordingly, Miyanaga fails to cure the deficiencies of

Hiroshima. Accordingly, Hiroshima in view of Miyanaga fails to teach or suggest each and every claimed feature of the present invention, as disclosed in amended claim 47.

Accordingly, Applicants respectfully request withdrawal of the 35 U.S.C. § 103(a) rejection of claim 47. Since none of the other prior art of record, whether taken alone or in any combination, discloses or suggests all the features of the claimed invention, Applicants respectfully submit that independent claim 47, and all the claims that depend therefrom, are allowable.

Allowable Subject Matter

Applicants appreciate the indication that claims 3, 4, 8, and 13 contain allowable subject matter. Claims 3, 4, 8, and 13 have been amended to address the aforementioned claim objections.

Accordingly, Applicants submit that claims 3, 4, 8, and 13 are in condition for allowance.

CONCLUSION

Applicants believe that a full and complete response has been made to the pending Office Action and respectfully submits that all of the stated objections and grounds for rejection have been overcome or rendered moot. Accordingly, Applicants respectfully submit that all pending claims are allowable and that the application is in condition for allowance.

Should the Examiner feel that there are any issues outstanding after consideration of this response, the Examiner is invited to contact the Applicants' undersigned representative at the number below to expedite prosecution.

Prompt and favorable consideration of this Reply is respectfully requested.

Respectfully submitted,

/hae-chan park/

Hae-Chan Park
Reg. No. 50,114

Date: July 17, 2006

CUSTOMER NUMBER: 58027
H.C. Park & Associates, PLC
8500 Leesburg Pike
Suite 7500
Vienna, VA 22182
Tel: 703-288-5105
Fax: 703-288-5139
HCP/BYC/kbs

EXHIBIT B

Monthly Statement of Deposit Account
for Deposit Account No. 50-3698

UNITED STATES PATENT AND TRADEMARK OFFICE

United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
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DATE POSTED MO.	DAY	YR.	CONTROL NO.	DESCRIPTION (Serial, Patent, TM, Order)	DOCKET NO.	FEE CODE	CHARGES/ CREDITS	BALANCE
7	11	06	662	10992645	61610347US	1252	450.00	4840.00
7	11	06	663	10992645	61610347US	1801	790.00	4050.00
7	12	06	3	11138320	61610570US	1202	50.00	4000.00
7	18	06	382	11457940	P1807USC2A	1011	300.00	3700.00
7	18	06	383	11457940	P1807USC2A	1111	500.00	3200.00
7	18	06	384	11457940	P1807USC2A	1311	200.00	3000.00
7	18	06	385	11457940	P1807USC2A	1201	400.00	2600.00
7	18	06	714	10617811	61610078US	1251	120.00	2480.00
7	25	06	2	10779781	6161.0111.US	1201	200.00	2280.00

AN AMOUNT SUFFICIENT TO COVER ALL SERVICES REQUESTED MUST ALWAYS BE ON DEPOSIT	OPENING BALANCE	TOTAL CHARGES	TOTAL CREDITS	CLOSING BALANCE
	5290.00	3010.00	0.00	2280.00

MS020D (5/2006)

*** O.D. INDICATES OVERDRAWN

EXHIBIT C

Fee Worksheet and Index of Claims

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 10/779,781

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))							
SEARCH FEE (37 CFR 1.16(k), (l), or (m))							
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))							
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 = *	*	x =		OR	x =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 = *	*	x =		OR	x =	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT A	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR		(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDI TIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDI TIONAL FEE ($)
Total (37 CFR 1.16(i))	47	Minus	** 47	=	0	x 25 =		OR	x 50 =	
Independent (37 CFR 1.16(h))	7	Minus	*** 6	=	1	x 100 =		OR	x 200 =	200
Application Size Fee (37 CFR 1.16(s))										
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
						TOTAL ADD'T FEE			TOTAL ADD'T FEE	

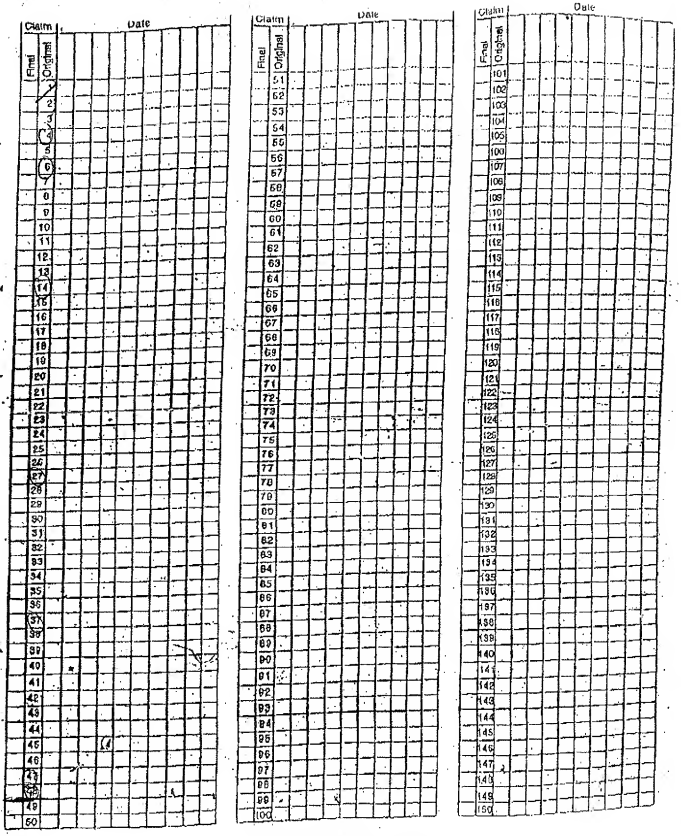
AMENDMENT B	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR		(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDI TIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDI TIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=		x =		OR	x =	
Independent (37 CFR 1.16(h))		Minus	***	=		x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))										
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
						TOTAL ADD'T FEE			TOTAL ADD'T FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.



If more than 150 claims or 10 actions
staple additional sheet here